UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,561	11/17/2003	Simon Charles Watt	550-486	5948

23117 7590 02/12/2007

NIXON & VANDERHYE, PC
901 NORTH GLEBE ROAD, 11TH FLOOR
ARLINGTON, VA 22203

EXAMINER	
FLOURNOY, HORACE L	
ART UNIT	PAPER NUMBER
2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/12/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/714,561	WATT ET AL.	
	Examiner	Art Unit	
	Horace L. Flournoy	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-50* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,25-32,49 and 50* is/are rejected.

7)☒ Claim(s) *9-24 and 33-48* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11/17/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

ACKNOWLEDGEMENT OF REFERENCES CITED BY APPLICANT

As required by M.P.E.P. 609(c), the applicant's submission of the Information Disclosure Statements dated **5/27/2005, 4/22/2004, 11/17/2003, and 1/16/2007** are acknowledged by the examiner and the cited references have been considered in the examination of the claims now pending. As required by M.P.E.P. 609(c), a copy of the PTOL-1449 initialed and dated by the examiner is attached to the instant office action.

REJECTIONS NOT BASED ON PRIOR ART

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

1. Claims **1-9 (also 10-18)** of U.S. application no. 10/714,520 contain every element of claims 1-9, 26-34, 49 and 50 of the instant application and as such anticipate claims 1-9, 26-34, 49 and 50 of the instant application.

2. Claim **4** of U.S. application no. 10/714,481 contains every element of claims 2, 26, 49 and 50 of the instant application and as such anticipates claims 2, 26, 49 and 50 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent

granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8, 25-32, 49 and 50 are rejected under 35 U.S.C. 102(e) as being anticipated by **Poisner (U.S. Patent Number 6,820,177 hereafter referred to as Poisner)**.

With respect to **independent claim 1,**

"A data processing apparatus having a secure domain and a non-secure domain **[See FIG. 1, elements 116 and 114, respectively]**, *in the secure domain the data processing apparatus having access to secure data which is not accessible in the non-secure domain* **[Poisner discloses this limitation, e.g. in column 2, lines 48-50]**, *the data processing apparatus comprising: a device bus* **[See FIG. 1, element 130: "Processor Bus"]**; *a device coupled to the device bus and operable to issue a memory access request pertaining to either said secure domain or said non-secure domain* **[See FIG. 1, element 110: "Processor"]**; *a memory coupled to the device bus and operable to store data required by the device* **[See FIG. 1, element 140: "Memory". The examiner notes that the memory is *coupled* to the device bus (processor bus) via the memory bus 150 and element 120.]**, *the memory comprising secure memory for storing secure data and non-secure memory for storing non-secure data* **[See FIG. 1, elements 141 and 142 which teach a "Protected" and a "Non-**

Protected" configuration space within the memory], *the device being operable to issue onto the device bus a memory access request when access to an item of data in the memory is required; and partition checking logic coupled to the device bus and operable whenever the memory access request as issued by the device pertains to said non-secure domain to detect if the memory access request is seeking to access the secure memory, and upon such detection to prevent the access specified by that memory access request"* **[Poisner discloses this limitation, in column 3 line 63- column 4, line 15.]**

With respect to **independent claim 25,**

"A method of controlling access to a memory in a data processing apparatus having a secure domain and a non-secure domain **[See FIG. 1, elements 116 and 114, respectively]**, *in the secure domain the data processing apparatus having access to secure data which is not accessible in the non-secure domain* **[Poisner discloses this limitation, e.g. in column 2, lines 48-50]**, *the data processing apparatus comprising a device bus* **[See FIG. 1, element 130: "Processor Bus"]**, *a device coupled to the device bus and operable to issue a memory access request pertaining to either said secure domain or said non-secure domain* **[See FIG. 1, element 110: "Processor"]**, *and a memory coupled to the device bus and operable to store data required by the device* **[See FIG. 1,**

element 140: "Memory". The examiner notes that the memory is *coupled* to the device bus (processor bus) via the memory bus 150 and element 120.], *the memory comprising secure memory for storing secure data and non-secure memory for storing non-secure data* **[See FIG. 1, elements 141 and 142 which teach a "Protected" and a "Non-Protected" configuration space within the memory]**, *the method comprising the steps of: (i) issuing from the device onto the device bus a memory access request when access to an item of data in the memory is required; and (ii) whenever the memory access request as issued by the device pertains to said non-secure domain, employing partition checking logic coupled to the device bus to detect if the memory access request is seeking to access the secure memory; and (iii) upon such detection, preventing the access specified by that memory access request."* **[Poisner discloses this limitation, in column 3 line 63-column 4, line 15.]**

Dependent Claims

With respect to **claims 2 and 26**,

"A data processing apparatus as claimed in Claim 1, wherein the device is operable in a plurality of modes, including at least one non-secure mode being a mode in the non-secure domain and at least one secure mode being a mode in the secure domain." **[Poisner discloses in column 3,**

lines 8-14, "FIG. 1 shows protected configuration space 141 and non-protected configuration space 142, which represent the ranges of addressable locations that are reserved for control and monitoring activities (protected and non-protected activities, respectively) that are implemented in logic circuit 120." The examiner interprets secure and non-secure modes as protected and non-protected activities]

With respect to **claims 3 and 27**,

"A data processing apparatus as claimed in Claim 1, wherein the partition checking logic is managed by the device when operating in a predetermined secure mode in said secure domain." **[disclosed in column 3, lines 8-14]**

With respect to **claims 4 and 28**,

"A data processing apparatus as claimed in Claim 1, wherein the memory access request issued by the device includes a domain signal identifying whether the memory access request pertains to said secure domain or said non-secure domain." **[Poisner discloses in column 8, lines 56-61, "Protected commands may be distinguished from non-protected commands in various ways. For example, 1) one or more control lines on the processor bus may be used to indicate whether the**

command is a protected command, 2) the data field may contain one or more bits indicating whether the command is a protected command..."]

With respect to **claims 5 and 29**,

"A data processing apparatus as claimed in Claim 4, wherein the device has a predetermined pin for outputting the domain signal onto the device bus." **[Poisner discloses in column 8, lines 56-61, "Protected commands may be distinguished from non-protected commands in various ways... 2) the data field may contain one or more bits indicating whether the command is a protected command..."]**

With respect to **claims 6 and 30**,

"A data processing apparatus as claimed in Claim 1, wherein the partition checking logic is provided within an arbiter **[Configuration space control logic disclosed in FIG. 1, element 124]** *coupled to the device bus to arbitrate between memory access requests issued on the device bus."* **[disclosed, e.g. in column 3, lines 48-62]**

With respect to **claims 7 and 31**,

"A data processing apparatus as claimed in Claim 1, wherein in said non-secure domain the device is operable under the control of a non-secure

operating system, and in said secure domain the device is operable under the control of a secure operating system." **[disclosed, e.g. in column 8, lines 32-36. See also column 1, lines 9-25.]**

With respect to **claims 8 and 32**,

"A data processing apparatus as claimed in Claim 1, wherein the device is a chip incorporating a processor, the chip further comprising a memory management unit operable, when the processor generates the memory access request, to perform one or more predetermined access control functions to control issuance of the memory access request onto the device bus." **[disclosed, e.g. in column 2, lines 30-60. The examiner notes that Poisner teaches separate processor units (See column 2, lines 35-37) which is interpreted as processors on their own respective chips]**

ALLOWABLE SUBJECT MATTER

Claims 2, 9-24, 26 and 33-48 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

CONCLUSION

Direction of Future Correspondences

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Horace L. Flournoy whose telephone number is (571) 272-2705. The examiner can normally be reached on Monday through Friday 8:00 AM to 5:30 PM (ET).

Important Note

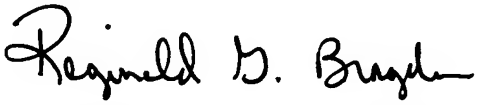
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald G. Bragdon can be reached on (571) 272-4204. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 746-7239.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have

questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-2100.

Reginald G. Bragdon



HLF
February 7th, 2007

Supervisory Patent Examiner
Technology Center 2100

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :5/27/05, 4/22/04, 11/17/03, 1/16/07.